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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
SOFOCLEOUS, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

	Application No.	Applicant(s)	
	10/788,581	COKER, THOMAS A.	
	Examiner	Art Unit	
	Alexander Sofocleous	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/27/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *(1) 5/9/2005*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☒ Other: *search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 27, 2004, and the Information Disclosure Statement filed on May 9, 2005.

2. Claims 1-29 are pending in the case. Claim 1, 3, 6, 9, 13, 17, 22, and 27 are independent claims.

Claim Objections

Claims 12, 16, 20, and 25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Independent claims 9, 13, 17, and 22, from which 12, 16, 20, and 25 depend respectively, are drawn to a volatile memory cell; whereas, claims 12, 16, 20, and 25 are drawn to a memory array containing the volatile memory cell and thereby broadens the scope of the invention.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3, and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Rastegar (U.S. Patent 5,297,094).**

Regarding independent claim 1 and 3, Rastegar '094 shows a circuit (Fig. 8) comprising a memory array (Fig. 8 [10]) comprising a plurality of memory cells, or at least one memory cell (Fig. 5), having first and second p-channel transistor (Fig. 5 [100]) and first and second n-channel transistors (Fig. 5 [96, 98]) in a cross-coupled latch configuration.

Rastegar '094 shows power control circuitry (Fig. 5 [Reset V_{SS}]) coupled to a source terminal of one of the n-channel transistors (Fig. 5 [98]) for providing to that source terminal a low voltage reference level during a normal mode of operation (column 7, lines 29-30) and transitioning that source terminal to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation (column 7, lines 32-33).

Regarding dependent claim 2, Rastegar '094 shows the source terminal (Fig. 5 [terminal of 96 connecting to V_{SS}]) of the other n-channel transistor (Fig. 5 [96]) is always coupled to the low voltage reference (Fig. 5 [V_{SS}]).

Regarding independent claim 13, Rastegar '094 shows a circuit (Fig. 8) comprising a volatile memory cell (Fig. 5) having a low reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]).

Rastegar '094 shows the circuit to comprise power control circuitry (Fig. 5 [Reset V_{SS}]) coupled to the volatile memory cell (Fig. 5) that transitions the low voltage reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) from a low voltage reference voltage associated with a normal mode of operation (column 7, lines 29-30) to a high voltage reference voltage in a data corruption mode (column 7, lines 32-33) and transitions the low voltage reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) from the high reference voltage back to the low voltage reference voltage.

As per **independent claim 9**, it encompasses the same scope of invention as to that of claim **13** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 14, Rastegar '094 shows the volatile memory cell comprises a 6T memory cell (see Fig. 5) and the low voltage reference terminal comprises a source terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) of one n-channel transistor (Fig. 5 [98]) in a latch portion of the memory cell.

As per **dependent claim 10**, it encompasses the same scope of invention as to that of claim **14** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 15, Rastegar '094 shows the source terminal (Fig. 5 [terminal of 96 connecting to V_{SS}]) of another n-channel transistor (Fig. 5 [96]) in the latch is always coupled to the low voltage reference (Fig. 5 [V_{SS}]).

As per **dependent claim 11**, it encompasses the same scope of invention as to that of claim **15** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

5. **Claims 1-3, and 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Rastegar (U.S. Patent 5,311,477).**

Regarding independent claim 1 and 3, Rastegar '477 shows a circuit (Fig. 8) comprising a memory array (Fig. 8 [10]) comprising a plurality of memory cells, or at least one memory cell (Fig. 5), having first and second p-channel transistor (Fig. 5 [100]) and first and second n-channel transistors (Fig. 5 [96, 98]) in a cross-coupled latch configuration.

Rastegar '477 shows power control circuitry (Fig. 5 [Reset V_{SS}]) coupled to a source terminal of one of the n-channel transistors (Fig. 5 [98]) for providing to that source terminal a low voltage reference level during a normal mode of operation (column 7, lines 11-12) and transitioning that source terminal to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation (column 7, lines 14-15).

Regarding dependent claim 2, Rastegar '477 shows the source terminal (Fig. 5 [terminal of 96 connecting to V_{SS}]) of the other n-channel transistor (Fig. 5 [96]) is always coupled to the low voltage reference (Fig. 5 [V_{SS}]).

Regarding independent claim 13, Rastegar '477 shows a circuit (Fig. 8) comprising a volatile memory cell (Fig. 5) having a low reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]).

Rastegar '477 shows the circuit to comprise power control circuitry (Fig. 5 [Reset V_{SS}]) coupled to the volatile memory cell (Fig. 5) that transitions the low voltage reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) from a low voltage reference voltage associated with a normal mode of operation (column 7, lines 11-12) to a high voltage reference voltage in a data corruption mode (column 7, lines 14-15) and transitions the low voltage reference terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) from the high reference voltage back to the low voltage reference voltage.

As per **independent claim 9**, it encompasses the same scope of invention as to that of claim **13** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 14, Rastegar '477 shows the volatile memory cell comprises a 6T memory cell (see Fig. 5) and the low voltage reference terminal comprises a source terminal (Fig. 5 [terminal of 98 connecting to Reset V_{SS}]) of one n-channel transistor (Fig. 5 [98]) in a latch portion of the memory cell.

As per **dependent claim 10**, it encompasses the same scope of invention as to that of claim **14** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 15, Rastegar '477 shows the source terminal (Fig. 5 [terminal of 96 connecting to V_{SS}]) of another n-channel transistor (Fig. 5 [96]) in the latch is always coupled to the low voltage reference (Fig. 5 [V_{SS}]).

As per **dependent claim 11**, it encompasses the same scope of invention as to that of claim **15** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

6. **Claims 1-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Rimondi et al. (U.S. Patent 6,963,499 B2).**

Regarding independent claim 1, and 3, Rimondi et al. show a circuit (Fig. 2) comprising a memory array (Fig. 2 [201]) comprising a plurality of memory cells, or at least one memory cell (Fig. 2 [101]; Fig. 1 [101]), having first and second p-channel transistors (Fig. 1 [P1, P2]) and first and second n-channel transistors (Fig. 1 [N1, N2]) in a cross-coupled latch configuration.

Rimondi et al. show the circuit to comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWb, GND, VDD]) coupled to the source terminal (Fig. 1 [SN2]) of one of the n-channel transistors (Fig. 1 [N2]) for providing to that source terminal a low voltage reference level during a normal mode of operation (column 3 lines 37-41) and transitioning that source terminal to a high voltage reference level and

back to the low voltage reference level during a data corruption mode of operation (column 4, lines 10-11, 16-18).

Regarding dependent claim 2 and 5, Rimondi et al. show the source terminal (Fig. 1 [SN1]) of the other n-channel transistor (Fig. 1 [N1]) is always coupled to the low voltage reference (Fig. 1 [GND]).

Regarding dependent claim 4, Rimondi et al. show the power control circuitry (Fig. 2 [209]) to comprise counter circuitry to sequentially select each group of memory cells so as to corrupt all memory cells (Fig. 2 [101]) in the memory array (Fig. 2 [201]).

Regarding independent claim 6 and 27, Rimondi et al. show a circuit (Fig. 2) comprising a memory array (Fig. 2 [201]) comprising a plurality of memory cells, or at least one memory cell (Fig. 2 [101]; Fig. 1 [101]), having first and second p-channel transistors (Fig. 1 [P1, P2]) and first and second n-channel transistors (Fig. 1 [N1, N2]) in a cross-coupled latch configuration.

Rimondi et al. show the circuit to comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWa, GND, VDD]) coupled to the source terminal (Fig. 1 [SP1]) of one of the p-channel transistors (Fig. 1 [P1]) for providing to that source terminal a high voltage reference level during a normal mode of operation (column 3 lines 37-41) and transitioning that source terminal to a low voltage reference level and back to the high voltage reference level during a data corruption mode of operation (column 4, lines 42-45).

Rimondi et al. show the circuit to further comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWb, GND, VDD]) coupled to the source terminal (Fig. 1

[SN2]) of one of the n-channel transistors (Fig. 1 [N2]) for providing to that source terminal a low voltage reference level during a normal mode of operation (column 3 lines 37-41) and transitioning that source terminal to a high voltage reference level and back to the low voltage reference level during a data corruption mode of operation (column 4, lines 10-11, 16-18).

Regarding dependent claim 7 and 28, Rimondi et al. show the source terminal (Fig. 1 [SN1]) of the other n-channel transistor (Fig. 1 [N1]) is always coupled to the low voltage reference (Fig. 1 [GND]).

Regarding dependent claim 8 and 29, Rimondi et al. show the power control circuitry (Fig. 2 [209]) transitions voltage on the source terminal (Fig. 1 [SP1]) of at least one p-channel transistor (Fig. 1 [P1]) and transitions voltage on the source terminal of the n-channel transistor (Fig. 1 [N2]) in an interleaved manner (see Fig. 2 [FCN1 and FC1]).

Regarding independent claim 13, Rimondi et al. show a circuit (Fig. 2) comprising a volatile memory cell (Fig. 2 [101]) having a low reference terminal (Fig. 1 [SN2]).

Rimondi et al. show the circuit to comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWb, GND, VDD]) coupled to the volatile memory cell (Fig. 2 [101]) that transitions the low voltage reference terminal (Fig. 1 [SN2]) from a low voltage reference voltage associated with a normal mode of operation (column 3 lines 37-41) to a high voltage reference voltage in a data corruption mode (column 4, lines 10-11, 16-18) and transitions the low voltage reference terminal

(Fig. 1 [SN2]) from the high reference voltage back to the low voltage reference voltage.

As per **independent claim 9**, it encompasses the same scope of invention as to that of claim **13** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 14, Rimondi et al. show the volatile memory cell comprises a 6T memory cell (see Fig. 1) and the low voltage reference terminal comprises a source terminal (Fig. 1 [SN2]) of one n-channel transistor (Fig. 1 [N2]) in a latch portion of the memory cell.

As per **dependent claim 10**, it encompasses the same scope of invention as to that of claim **14** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 15, Rimondi et al. show the source terminal (Fig. 1 [SN1]) of another n-channel transistor (Fig. 1 [N1]) in the latch is always coupled to the low voltage reference (Fig. 1 [GND]).

As per **dependent claim 11**, it encompasses the same scope of invention as to that of claim **15** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 16, Rimondi et al. show a memory array (Fig. 2 [201]) including a plurality of volatile memory cells (Fig. 2 [101]), the memory cells arranged in a plurality of groups, the power control circuitry (Fig. 2

[209]) selectively transitioning, one group at a time, the low voltage reference terminals (Fig. 2 [SN2]) for the memory cells in the selected group (see Fig. 2).

As per **independent/dependent claim 12**, it encompasses the same scope of invention as to that of claim **16** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding independent claim 22, Rimondi et al. show a circuit (Fig. 2) comprising a volatile memory cell (Fig. 2 [101]) having a low voltage reference terminal (Fig. 1 [SN2]) and a high voltage reference terminal (Fig. 1 [SP1]).

Rimondi et al. show the circuit to comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWa, GND, VDD]) coupled to the volatile memory cell (Fig. 2 [101]) that transitions the high voltage reference terminal (Fig. 1 [SP1]) from a high voltage reference voltage associated with a normal mode of operation (column 3 lines 37-41) to a low voltage reference voltage in a data corruption mode (column 4, lines 42-45) and transitions the high voltage reference terminal (Fig. 1 [SP1]) from the high reference voltage back to the low voltage reference voltage.

Rimondi et al. show the circuit to comprise power control circuitry (Fig. 2 [209]; Fig. 1 [SWb, GND, VDD]) coupled to the volatile memory cell (Fig. 2 [101]) that transitions the low voltage reference terminal (Fig. 1 [SN2]) from a low voltage reference voltage associated with a normal mode of operation (column 3 lines 37-41) to a high voltage reference voltage in a data corruption mode (column 4, lines 10-11, 16-18) and transitions the low voltage reference terminal

(Fig. 1 [SN2]) from the high reference voltage back to the low voltage reference voltage.

As per **independent claim 17**, it encompasses the same scope of invention as to that of claim **22** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 23, Rimondi et al. show the volatile memory cell comprises a 6T memory cell (see Fig. 1) and the low voltage reference terminal comprises a source terminal (Fig. 1 [SN2]) of one n-channel transistor (Fig. 1 [N2]) in a latch portion of the memory cell and the high voltage reference terminal comprises a source terminal (Fig. 1 [SP1]) of at least one p-channel transistor (Fig. 1 [P1]) in the latch portion of the memory cell.

As per **dependent claim 18**, it encompasses the same scope of invention as to that of claim **23** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 24, Rimondi et al. show the source terminal (Fig. 1 [SN1]) of another n-channel transistor (Fig. 1 [N1]) in the latch is always coupled to the low voltage reference (Fig. 1 [GND]).

As per **dependent claim 19**, it encompasses the same scope of invention as to that of claim **24** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 25, Rimondi et al. show the volatile memory cell is part of a memory array (Fig. 2 [201]) including a plurality of like volatile

memory cells (Fig. 2 [101]), the power control circuitry (Fig. 2 [209]) transitioning the low voltage reference terminals (Fig. 2 [SN2]) and the high voltage reference terminals (Fig. 2 [SP1]) for all memory cells.

As per **dependent claim 20**, it encompasses the same scope of invention as to that of claim **25** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Regarding dependent claim 26, Rimondi et al. shows that the power control circuitry (Fig. 2 [209]) transitions voltage on the low and high voltage reference terminals in an interleaved manner (see Fig. 2 [FCN1 and FC1]).

As per **dependent claim 21**, it encompasses the same scope of invention as to that of claim **26** except it drafts in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Landeta et al. (U.S. Patent 5,373,466), Hsieh et al. (U.S. Patent 5,774,411), and Ito et al. (U.S. Patent 5,5159,571).

Landeta et al. show a flash clear method.

Hsieh et al show a cross-coupled memory cell where the source terminals of the n-channel transistors are connected to a negative voltage source.

Ito et al. show a cross-coupled memory cell with switching circuitry on the source terminal of the p-channel transistors.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on M-F 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

VAN THU NGUYEN
PRIMARY EXAMINER